Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A microprocessor having an instruction cache for providing a plurality of instruction bytes in response to a fetch address, the microprocessor also having a branch predictor for predicting in response to the fetch address whether a branch instruction is present in the plurality of instruction bytes provided by the instruction cache and for providing a prediction of whether or not the branch instruction will be taken, the microprocessor also having branch control logic that provides an indication of whether or not the microprocessor fetched a plurality of instruction bytes from the instruction cache at a target address of the branch instruction in response to the prediction, comprising:

an instruction buffer, comprising a plurality of stages each for buffering a plurality of instruction bytes received from ~~an~~ the instruction cache;

a branch indicator associated with each of said plurality of stages, for storing ~~an~~ the indication of whether or not the microprocessor ~~branched to a~~ fetched a plurality of instruction bytes for storage in said instruction buffer from the instruction cache at the target address of ~~a~~ the branch instruction buffered in said associated stage; ~~and~~

instruction format logic, for examining said plurality of instruction bytes stored in a first at least one of said plurality of instruction buffer stages during a first clock cycle, for outputting a length of an instruction currently being formatted by said instruction format logic comprised in said first at least one of said plurality of instruction buffer stages, and for examining said plurality of instruction bytes stored in a second at least one of said plurality of instruction buffer stages during a second clock cycle subsequent to said first clock cycle;

a multiplexer, coupled ~~to~~ between said instruction buffer and said instruction format logic, for selecting ~~one~~ said first at least one of said plurality of

stages for said instruction format logic to examine during said first clock cycle, and for selecting said second at least one of said plurality of stages for said instruction format logic to examine during said second clock cycle based on said branch indicator associated with ~~one~~ said first at least one of said plurality of stages and based on said length of said currently formatted instruction output by said instruction format logic; and

a wrap indicator, coupled to said multiplexer, for indicating whether or not said currently formatted instruction wraps across two of said first at least one of said plurality of instruction buffer stages, based on said currently formatted instruction length;

wherein if said branch indicator indicates the microprocessor fetched a plurality of instruction bytes from the instruction cache at the target address of the branch instruction, then said multiplexer selects said second at least one of said plurality of stages for said instruction format logic to examine during said second clock cycle based on whether said wrap indicator indicates said branch instruction wrapped across two of said first at least one of said plurality of instruction buffer stages.

2-7. (canceled)

8. (currently amended) The microprocessor of claim ~~7~~ 1, wherein if said branch indicator indicates the microprocessor fetched a plurality of instruction bytes from the instruction cache at the target address of the branch instruction ~~branched~~, then if said wrap indicator indicates that said branch instruction wrapped across two of said first at least one of said plurality of instruction buffer stages ~~beyond said bottom stage~~, then said multiplexer selects said second at least one of said plurality of stages for said instruction format logic to examine during said second clock cycle ~~one of said plurality of stages~~ two above said first at least one of said plurality of stages~~bottom stage~~.

9. (currently amended) The microprocessor of claim 8, wherein said instruction buffer shifts out two of said plurality of stages during a third clock cycle subsequent to said second clock cycle.

10. (currently amended) The microprocessor of claim 8, wherein if said branch indicator indicates the microprocessor fetched a plurality of instruction bytes from the instruction cache at the target address of the branch instruction ~~branched~~, then if said wrap indicator indicates that said branch instruction did not wrap across two of said first at least one of said plurality of instruction buffer stages ~~beyond said bottom stage~~, then said multiplexer selects said second at least one of said plurality of stages for said instruction format logic to examine during said second clock cycle ~~one of said plurality of stages~~ one above said first at least one of said plurality of stages~~bottom stage~~.

11. (currently amended) The microprocessor of claim 10, wherein said instruction buffer shifts out one of said plurality of stages during a third clock cycle subsequent to said second clock cycle.

12. (currently amended) The microprocessor of claim 10, further comprising:

a carry indicator, coupled to said multiplexer, for indicating whether or not a byte of said currently formatted instruction occupies a last byte of a lowest one of said first at least one of said plurality of stages ~~said bottom stage~~, based on said currently formatted instruction length.

13. (currently amended) The microprocessor of claim 12, wherein if said branch indicator indicates the microprocessor did not fetch a plurality of instruction bytes from the instruction cache at the target address of the branch instruction ~~branch~~, then said multiplexer selects said second at least one of said plurality of stages for said instruction format logic to examine during said second clock cycle ~~one of said plurality of stages~~ based on whether or not said carry indicator indicates said currently formatted instruction occupies a last byte of said lowest one of said first at least one of said plurality of stages~~bottom stage~~.

14. (currently amended) The microprocessor of claim 13, wherein if said branch indicator indicates the microprocessor did not fetch a plurality of instruction bytes from the instruction cache at the target address of the branch instruction ~~branch~~, then if said carry indicator indicates said currently formatted instruction occupies a last byte of said lowest one of said first at least one of said plurality of stages ~~bottom stage~~, then said multiplexer selects said second at least one of said plurality of stages for said instruction format logic to examine during said second clock cycle ~~one of said plurality of stages~~ one above said first at least one of said plurality of stages ~~bottom stage~~.

15. (currently amended) The microprocessor of claim 14, wherein said instruction buffer shifts out one of said plurality of stages during a third clock cycle subsequent to said second clock cycle.

16. (currently amended) The microprocessor of claim 14, wherein if said branch indicator indicates the microprocessor did not fetch a plurality of instruction bytes from the instruction cache at the target address of the branch instruction ~~branch~~, then if said carry indicator indicates said instruction does not occupy a last byte of said lowest one of said first at least one of said plurality of stages ~~bottom stage~~, then said multiplexer selects said first at least one of said plurality of stages ~~bottom stage~~.

17. (currently amended) The microprocessor of claim 16, wherein said instruction buffer shifts out none of said plurality of stages during a third clock cycle subsequent to said second clock cycle.

18-50. (canceled)